

General Description

Switching regulator and DC-DC Converter applications.

It is mainly suitable for Back-light Inverter.

FEATURES

□N-Channel

: $V_{DS}=30V$, $I_D=7A$.

: $R_{DS(ON)}=23.5m\Omega$ (Max.) @ $V_{GS}=10V$

: $R_{DS(ON)}=39m\Omega$ (Max.) @ $V_{GS}=4.5V$

□P-Channel

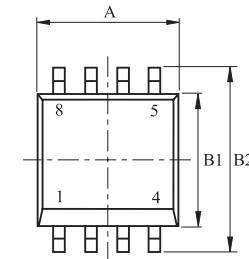
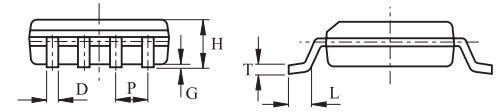
: $V_{DS}=-30V$, $I_D=-5A$.

: $R_{DS(ON)}=45.5m\Omega$ (Max.) @ $V_{GS}=-10V$

: $R_{DS(ON)}=80m\Omega$ (Max.) @ $V_{GS}=-4.5V$

□Super High Dense Cell Design.

□Reliable and rugged.



DIM	MILLIMETERS
A	4.85 ± 0.2
B1	3.94 ± 0.2
B2	6.02 ± 0.3
D	0.4 ± 0.1
G	$0.15+0.1/-0.05$
H	1.63 ± 0.2
L	0.65 ± 0.2
P	1.27
T	$0.20+0.1/-0.05$

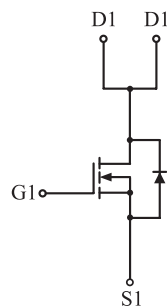
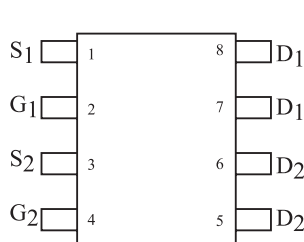
FLP-8

MAXIMUM RATING ($T_a=25^\circ C$)

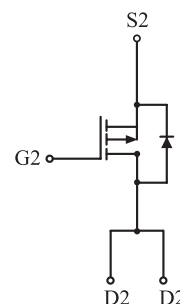
CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 10	± 20	V
Drain Current	DC	I_D^*	7	-5	A
	Pulsed (note1)	I_{DP}	29	-7	A
Source-Drain Diode Current		I_S	1.7	-1.7	A
Drain Power Dissipation		P_D^*	2		W
Maximum Junction Temperature		T_j	150		$^\circ C$
Storage Temperature Range		T_{stg}	$-55 \sim 150$		$^\circ C$
Thermal Resistance, Junction to Ambient		R_{thJA}^*	62.5		$^\circ C/W$

Note : *Surface Mounted on FR4 Board

PIN CONNECTION (TOP VIEW)



N-Channel MOSFET



P-Channel MOSFET

KMB7D0NP30QA

ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V,	N-Ch	30	-	-	V
		I _D =-250μA, V _{GS} =0V,	P-Ch	-30	-	-	
Drain Cut-off Current	I _{DSS}	V _{GS} =0V, V _{DS} =24V	N-Ch	-	-	1	μA
		V _{GS} =0V, V _{DS} =-24V	P-Ch	-	-	-1	
Gate Leakage Current	I _{GSS}	V _{GS} =± 20V, V _{DS} =0V	N-Ch	-	-	± 100	nA
			P-Ch	-	-	± 100	
Gate Threshold Voltage	V _{th}	V _{DS} =V _{GS} , I _D =250μA	N-Ch	1.0	-	3	V
		V _{DS} =V _{GS} , I _D =-250μA	P-Ch	-1.0	-	-3	
Drain-Source ON Resistance	r _{DS(on)}	V _{GS} =10V, I _D =7A	N-Ch	-	18	23.5	mΩ
		V _{GS} =-10V, I _D =-5A	P-Ch	-	35	45.5	
		V _{GS} =4.5V, I _D =6A	N-Ch	-	30	39	
		V _{GS} =-4.5V, I _D =-4A	P-Ch	-	62	80	
ON State Drain Current	I _{DS(on)} *	V _{GS} =10V, V _{DS} =5V	N-Ch	20	-	-	A
		V _{GS} =-10V, V _{DS} =-5V	P-Ch	-20	-	-	
Forward Transconductance	g _{fs} *	V _{GS} =5V, I _D =6.6A	N-Ch	-	10	-	S
		V _{GS} =-5V, I _D =-5A	P-Ch	-	9	-	
Source-Drain Diode Forward Voltage	V _{SD} *	I _S =1.7A, V _{GS} =0V	N-Ch	-	0.7	1.2	V
		I _S =-1.7A, V _{GS} =0V	P-Ch	-	0.8	-1.2	

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ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Dynamic							
Total Gate Charge	Q _g	N-Ch : V _{DS} =15V, I _D =6.6A, V _{GS} =10V (Fig.1)	N-Ch	-	16.4	nC	
		P-Ch : V _{DS} =-15V, I _D =-5A, V _{GS} =-10V (Fig.3)	P-Ch	-	13		16
		N-Ch : V _{DS} =15V, I _D =6.6A, V _{GS} =4.5V (Fig.1)	N-Ch	-	7.2		9
		P-Ch : V _{DS} =-15V, I _D =-5A, V _{GS} =-4.5V (Fig.3)	P-Ch	-	6.25		7.8
Gate-Source Charge	Q _{gs}	N-Ch : V _{DS} =15V, I _D =6.6A, V _{GS} =10V (Fig.1)	N-Ch	-	4	-	
Gate-Drain Charge	Q _{gd}	P-Ch : V _{DS} =-15V, I _D =-5A, V _{GS} =-10V (Fig.3)	P-Ch	-	2.6	-	
			N-Ch	-	2.6	-	
Turn-on Delay time	t _{d(on)}	N-Ch : V _{DS} =15V, I _D =6.6A, V _{GS} =10V, R _G =3Ω (Fig.2) P-Ch : V _{DS} =-15V, I _D =-5A, V _{GS} =-10V, R _G =3Ω, R _L =2Ω (Fig.4)	N-Ch	-	7.4	-	ns
			P-Ch	-	4.7	-	
Turn-on Rise time	t _r		N-Ch	-	27.7	-	
	P-Ch		-	7.8	-		
Turn-off Delay time	t _{d(off)}		N-Ch	-	12.2	-	
	P-Ch		-	47.2	-		
Turn-off Fall time	t _f		N-Ch	-	7.6	-	
	P-Ch		-	22.6	-		
Input Capacitance	C _{iss}	N-Ch : V _{DS} =15V, V _{GS} =0V, f=1.0MHz P-Ch : V _{DS} =-15V, V _{GS} =0V, f=1.0MHz	N-Ch	-	742	-	pF
Output Capacitance	C _{oss}		P-Ch	-	820	-	
			N-Ch	-	126	-	
Reverse transfer Capacitance	C _{rss}		P-Ch	-	137	-	
			N-Ch	-	76	-	
		P-Ch	-	89	-		

Note 1>* Pulse test : Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

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N-Channel

Fig1. $I_D - V_{DS}$

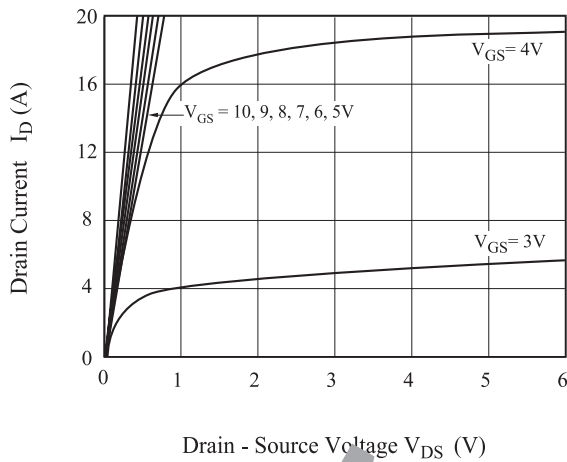


Fig2. $I_D - V_{GS}$

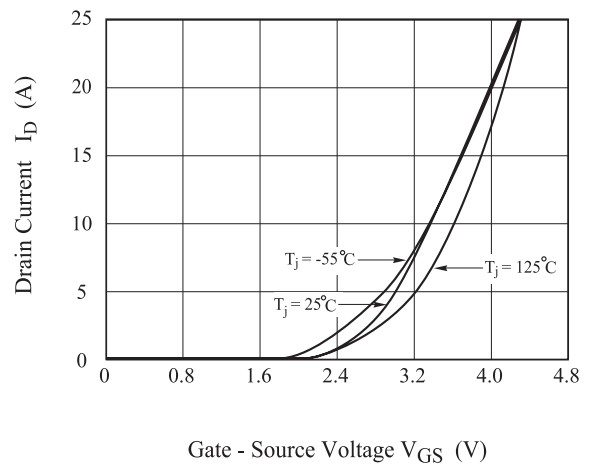


Fig3. V_{th}

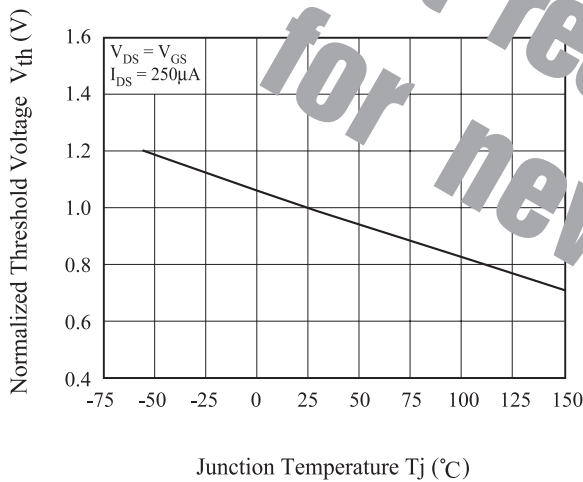


Fig4. $I_{DR} - V_{SD}$

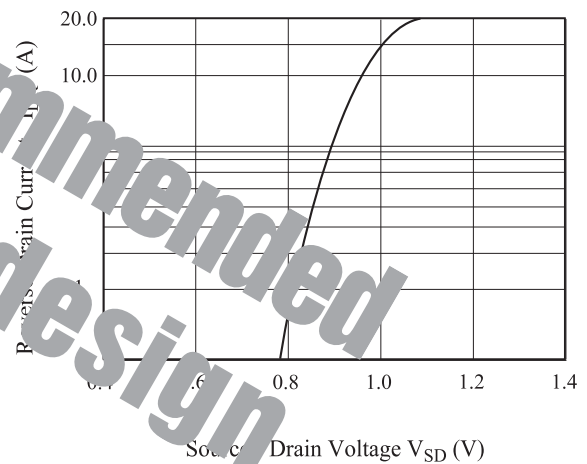


Fig5. $R_{DS(ON)} - T_j$

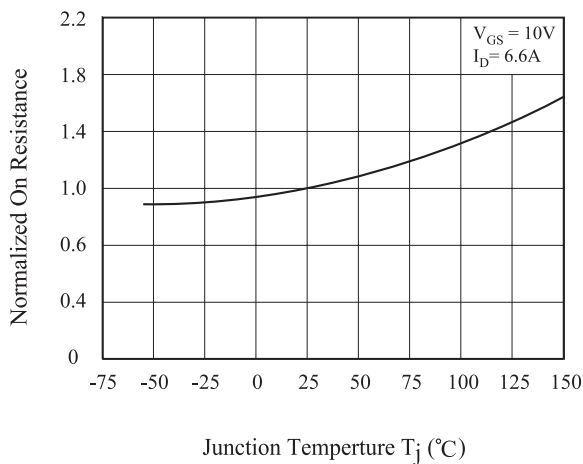
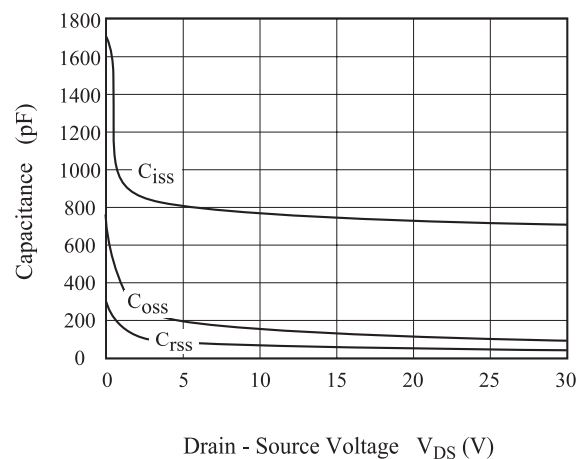


Fig6. $C - V_{DS}$



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Fig7. $Q_g - V_{GS}$

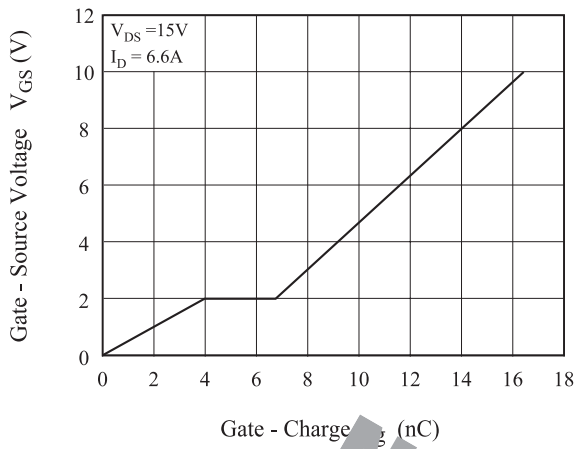


Fig8. Safe Operation Area

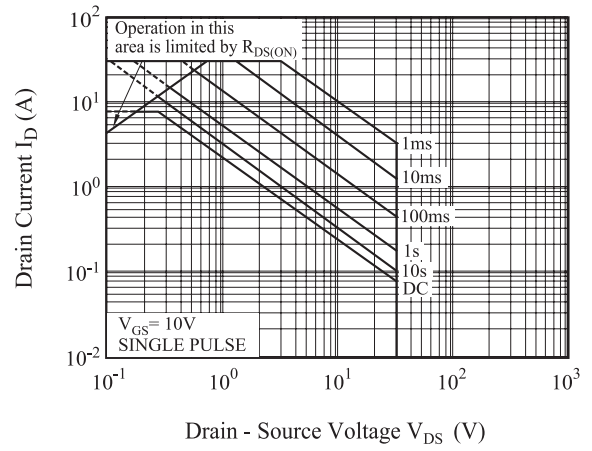
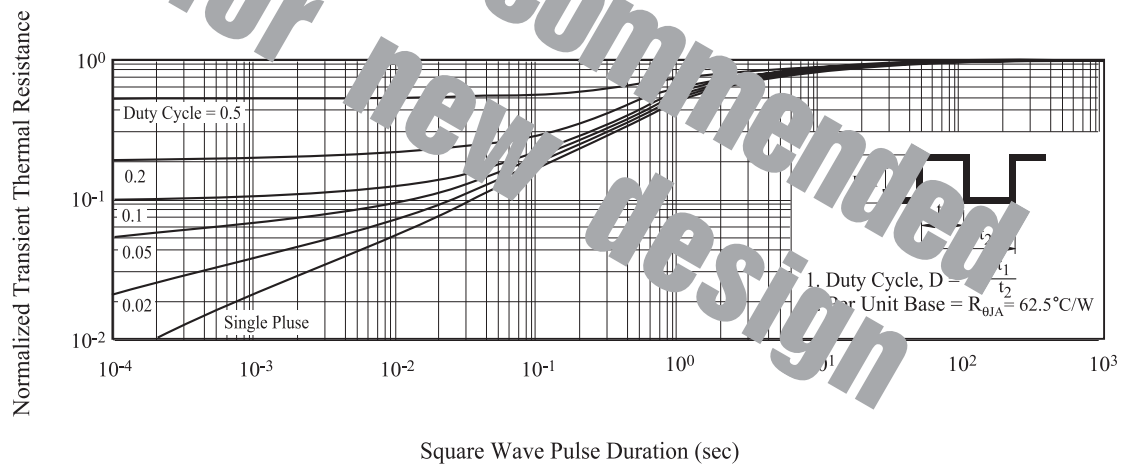


Fig9. Transient Thermal Response Curve



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P-Channel

Fig1. $I_D - V_{DS}$

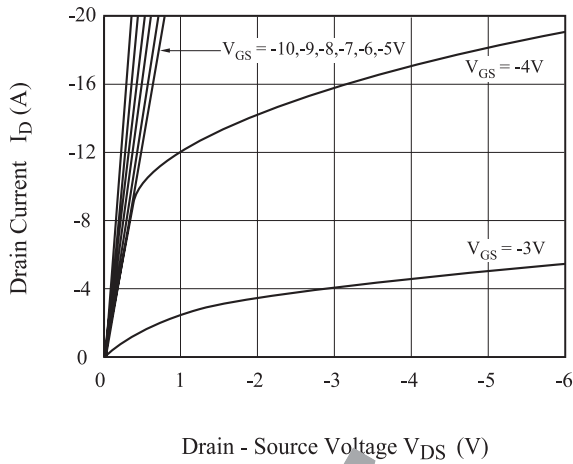


Fig2. $I_D - V_{GS}$

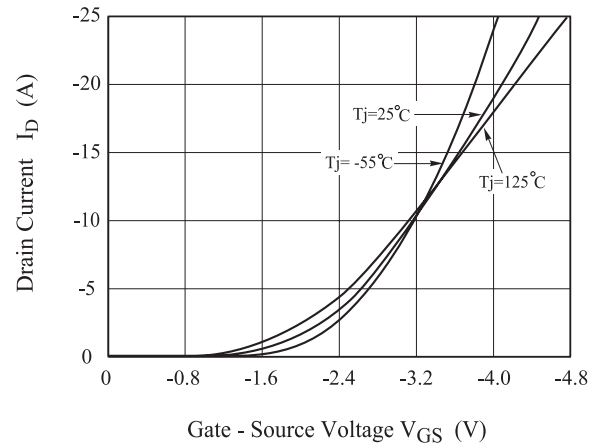


Fig3. $V_{th} - T_J$

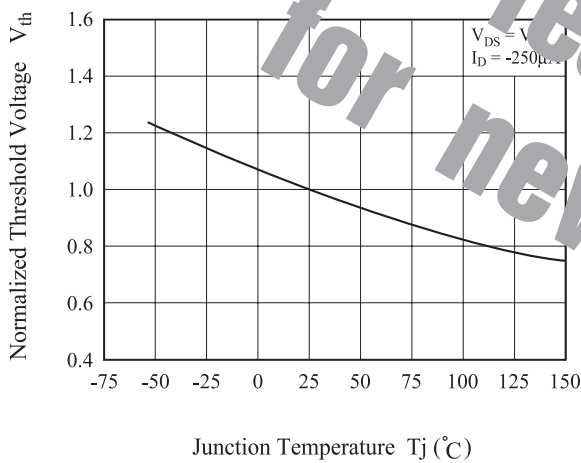


Fig4. $I_{DR} - V_{SD}$

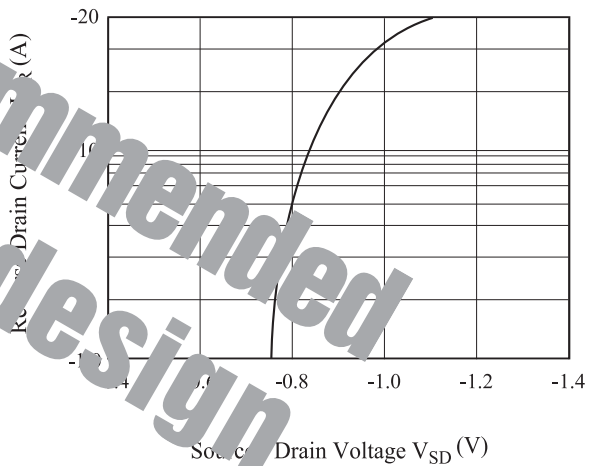


Fig5. $R_{DS(ON)} - T_J$

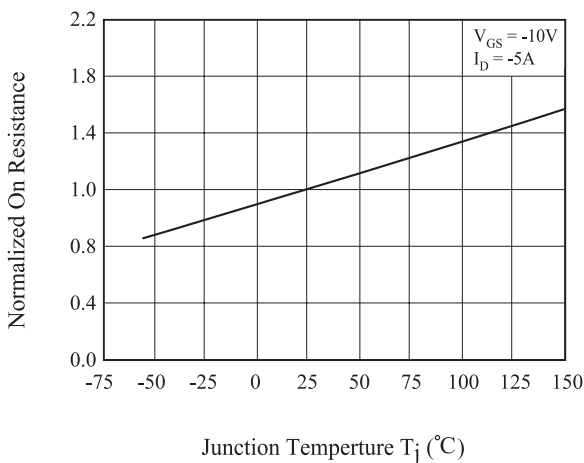
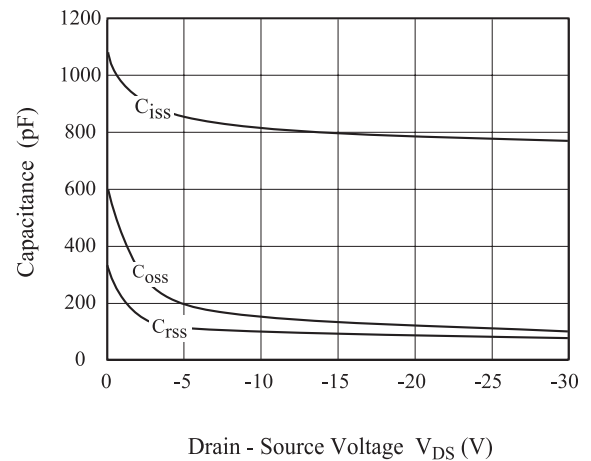


Fig6. $C - V_{DS}$



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Fig7. $Q_g - V_{GS}$

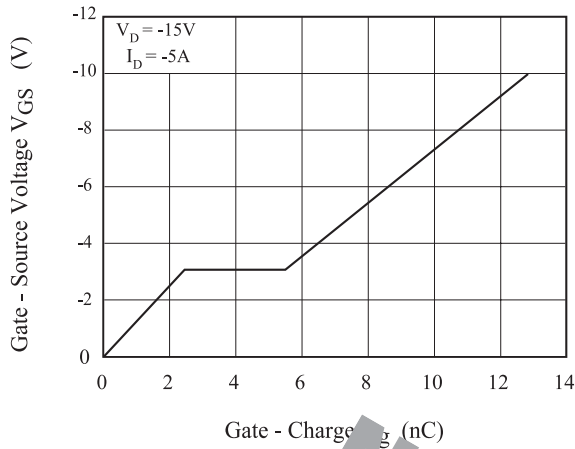


Fig8. Safe Operation Area

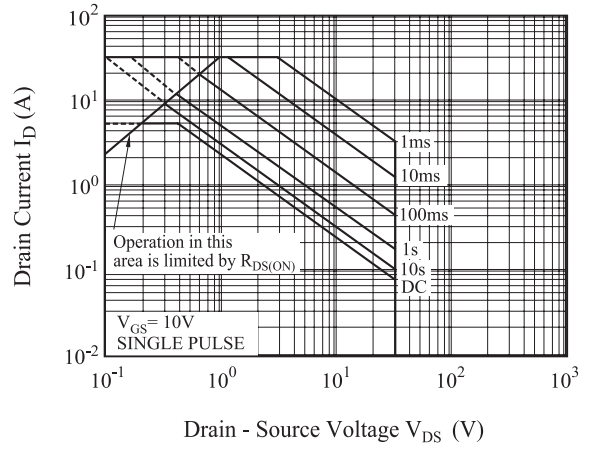
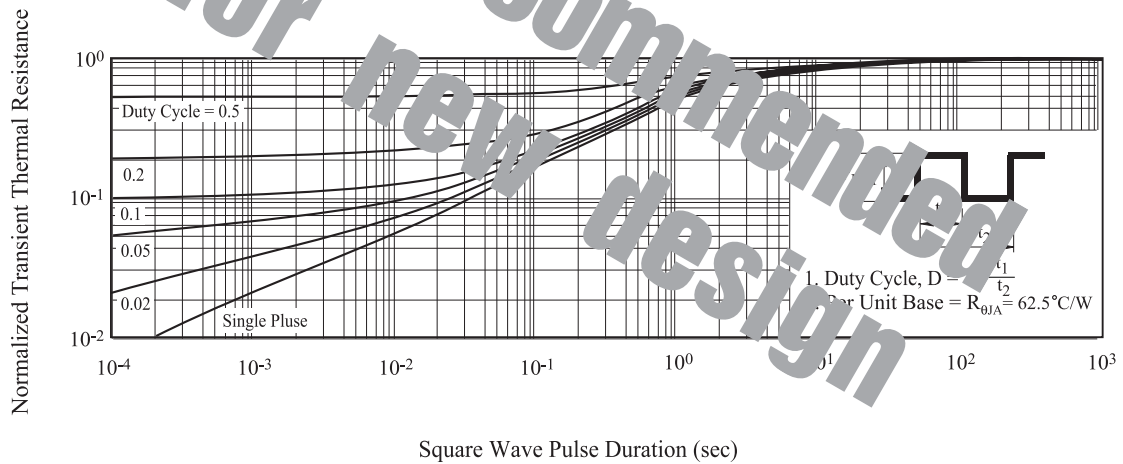


Fig9. Transient Thermal Response Curve



N-Channel

Fig. 1 Gate Charge

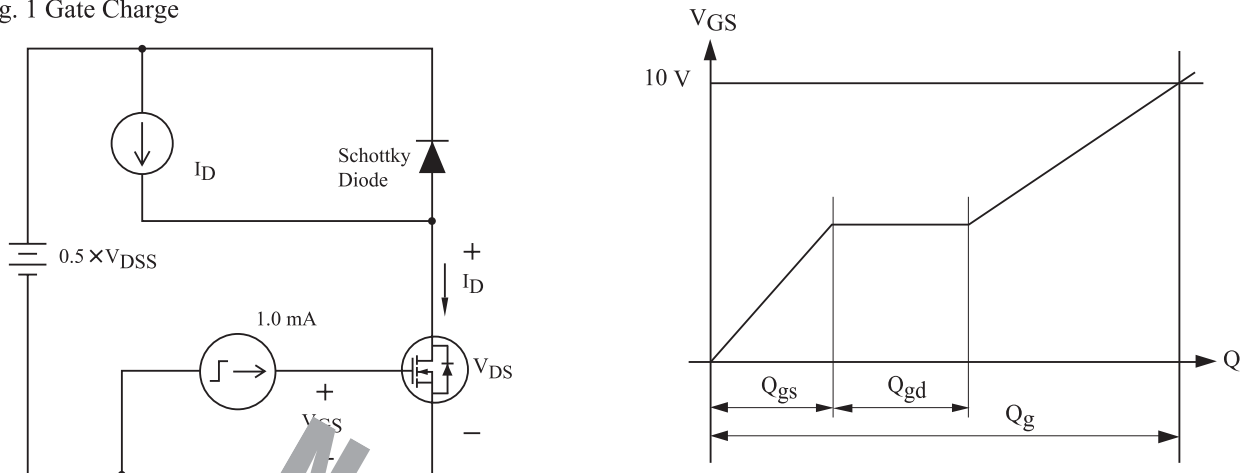
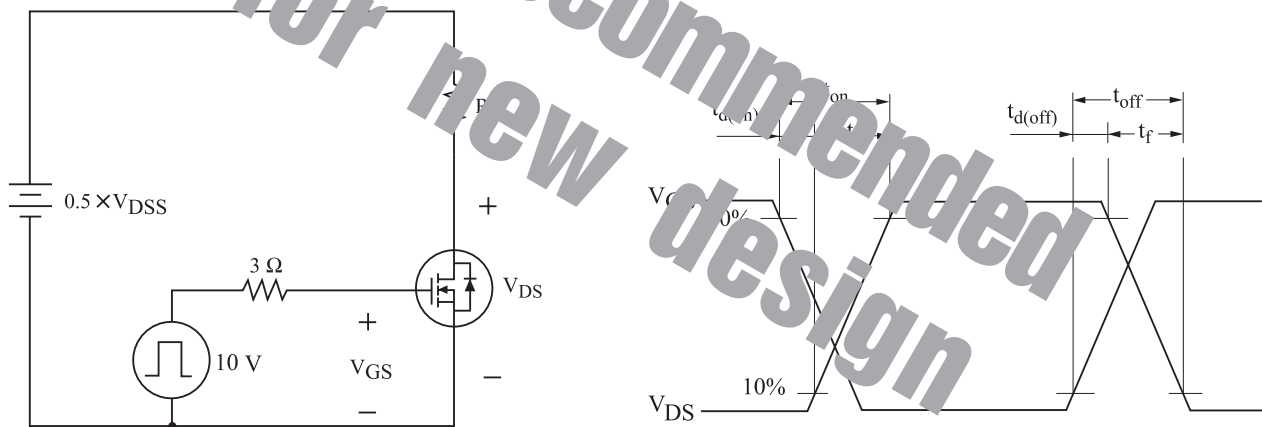


Fig. 2 Resistive Load Switching



P-Channel

Fig. 1 Gate Charge

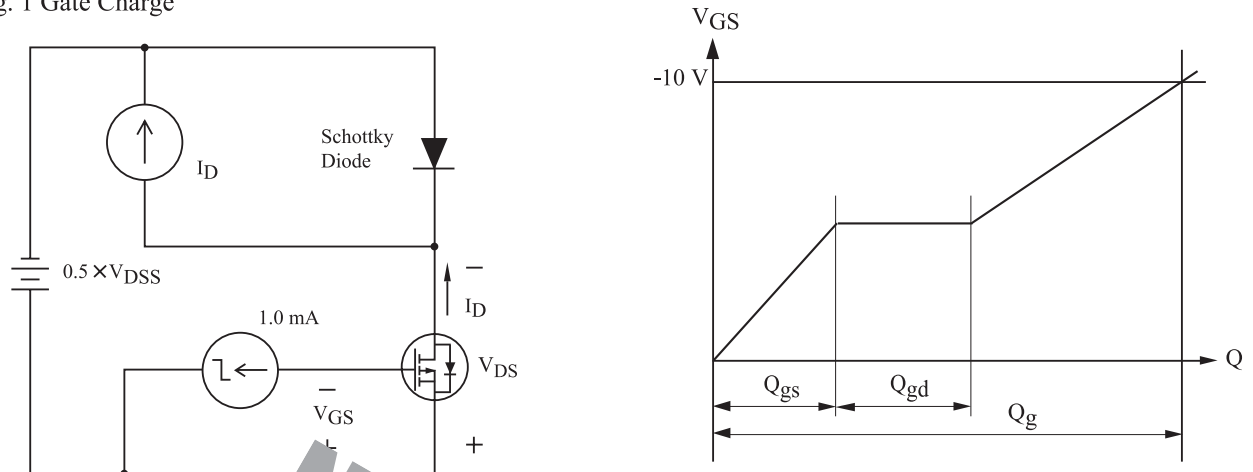
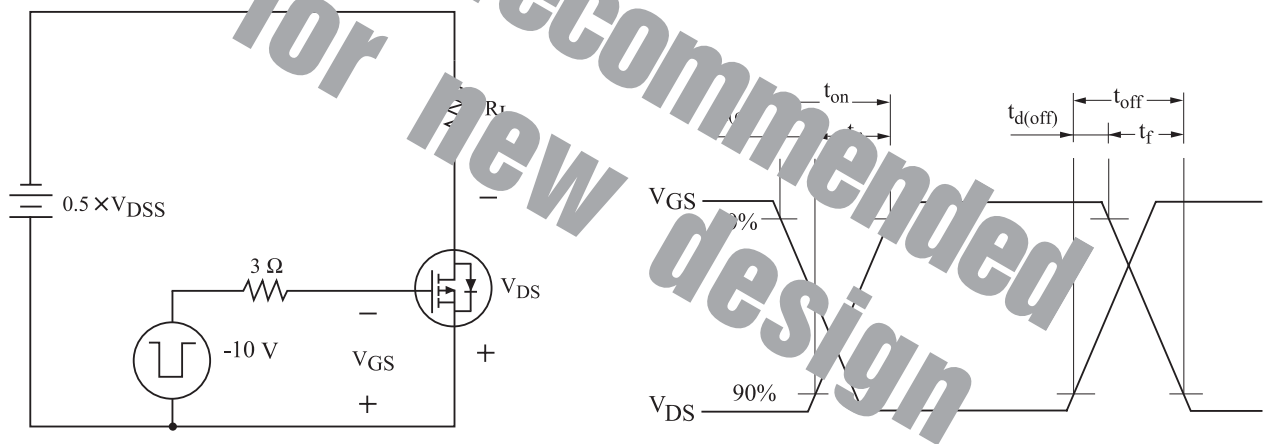


Fig. 2 Resistive Load Switching



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